

**IN THE CLAIMS:**

Each of claims 1 through 7, 9 through 24 and 26 through 44 has been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

**Listing of Claims:**

1. (currently amended) A method for interconnecting at least two semiconductor dice, comprising:  
providing a first semiconductor die including a plurality of bond pads arranged in an array over an active surface thereof;  
providing at least one second semiconductor die including a plurality of bond pads on an active surface thereof, ~~at least one of said first and said at least one second semiconductor dice including recessed bond pads;~~  
orienting ~~said the~~ first semiconductor die and ~~said the~~ at least one second semiconductor die with ~~said the~~ active surfaces thereof facing each other by aligning a peripheral edge of the at least one second semiconductor die with an alignment structure disposed on the active surface of the first semiconductor die, ~~with said the~~ at least one second semiconductor die covering some bond pads of ~~said the~~ plurality of bond pads, other bond pads of ~~said the~~ plurality of bond pads remaining exposed beyond an outer periphery of ~~said the~~ at least one second semiconductor die;  
electrically connecting ~~said the~~ some bond pads with corresponding bond pads of ~~said the~~ plurality of bond pads of ~~said the~~ first semiconductor die, ~~said recessed bond pads at least partially receiving conductive structures for connection with corresponding bond pads to facilitate alignment of said recessed bond pads and said corresponding bond pads.~~

2. (currently amended) The method of claim 1, wherein ~~said~~ providing ~~said~~ the first semiconductor die comprises providing a logic device.

3. (currently amended) The method of claim 2, wherein ~~said~~ providing ~~said~~ the at least one second semiconductor die comprises providing at least one memory device.

4. (currently amended) The method of claim 1, wherein ~~said~~ electrically connecting comprises providing conductive structures directly between each of ~~said~~ the plurality of bond pads of ~~said~~ the at least one second semiconductor die and ~~said~~ the corresponding bond pads of ~~said~~ the first semiconductor die.

5. (currently amended) The method of claim 4, wherein ~~said~~ providing conductive structures comprises providing balls, bumps, columns, or pillars comprising conductive material.

6. (currently amended) The method of claim 4, wherein ~~said~~ providing conductive structures comprises providing structures formed from a material comprising at least one of a metal, an alloy, a conductive epoxy, and a conductor-filled epoxy.

7. (currently amended) The method of claim 1, further comprising aligning ~~said~~ the at least some bond pads of ~~said~~ the at least one second semiconductor die with ~~said~~ the corresponding bond pads of ~~said~~ the first semiconductor die.

8. (canceled)

9. (currently amended) The method of claim 1, further comprising:  
providing a carrier including a plurality of contacts;  
orienting ~~said~~ the first semiconductor die with ~~said~~ the active surface thereof facing ~~said~~ the carrier; and

electrically connecting ~~said~~ the other bond pads of ~~said~~ the first semiconductor die to corresponding contacts of ~~said~~ the carrier.

10. (currently amended) The method of claim 9, wherein ~~said~~ providing ~~said~~ the carrier comprises providing a carrier substrate with ~~said~~ the plurality of contacts comprising contact pads located on a surface thereof.

11. (currently amended) The method of claim 10, wherein ~~said~~ providing ~~said~~ the carrier substrate comprises providing ~~said~~ the carrier substrate with at least one recess formed in ~~said~~ the surface.

12. (currently amended) The method of claim 11, wherein ~~said~~ orienting includes at least partially disposing at least ~~said~~ the at least one second semiconductor die in ~~said~~ the at least one recess.

13. (currently amended) The method of claim 9, wherein ~~said~~ providing ~~said~~ the carrier comprises providing leads corresponding to each of ~~said~~ the other bond pads.

14. (currently amended) The method of claim 9, wherein ~~said~~ electrically connecting ~~said~~ the other bond pads of ~~said~~ the first semiconductor die to ~~said~~ the corresponding contacts of ~~said~~ the carrier comprises disposing conductive elements between ~~said~~ the other bond pads and ~~said~~ the corresponding contacts.

15. (currently amended) The method of claim 14, wherein ~~said~~ disposing conductive elements comprises providing at least one of balls, bumps, columns, and pillars comprising conductive material between each of ~~said~~ the other bond pads and ~~said~~ the corresponding contacts.

16. (currently amended) The method of claim 14, wherein ~~said~~ disposing ~~said~~ the conductive elements between ~~said~~ the other bond pads of ~~said~~ the first semiconductor die and ~~said~~ the corresponding contacts of ~~said~~ the carrier comprises providing a quantity of a material comprising at least one of a metal, an alloy, a conductive epoxy, and a conductor-filled epoxy.

17. (currently amended) The method of claim 10, wherein ~~said~~ providing ~~said~~ the first semiconductor die comprises providing ~~said~~ the first semiconductor die with a first member of a conductive element secured to each other bond pad thereof and wherein ~~said~~ providing ~~said~~ the carrier substrate comprises providing ~~said~~ the carrier substrate with a second member of ~~said~~ the conductive element secured to each corresponding contact pad thereof.

18. (currently amended) The method of claim 17, further comprising aligning at least ~~said~~ the first and second members of ~~said~~ the conductive element.

19. (currently amended) The method of claim 18, further comprising securing at least ~~said~~ the first and second members of ~~said~~ the conductive element directly to each other.

20. (currently amended) The method of claim 17, further comprising providing a conductive mating structure bearing a third member of ~~said~~ the conductive element between ~~said~~ the first semiconductor die and ~~said~~ the carrier substrate.

21. (currently amended) The method of claim 20, further comprising aligning ~~said~~ the first, second, and third members of ~~said~~ the conductive element.

22. (currently amended) The method of claim 21, further comprising securing ~~said~~ the first, second, and third members of ~~said~~ the conductive element to one another.

23. (currently amended) A method for packaging a semiconductor device assembly, comprising:

providing a first semiconductor die including a plurality of bond pads arranged in an array over an active surface thereof;

providing at least one second semiconductor die including a plurality of bond pads arranged on an active surface thereof, ~~said plurality of bond pads of at least one of said first semiconductor die and said at least one second semiconductor die being recessed relative to an active surface thereof to facilitate subsequent alignment of corresponding bond pads of said first semiconductor die and said at least one second semiconductor die;~~

orienting ~~said the~~ at least one second semiconductor die over ~~said the~~ first semiconductor die with ~~said the~~ active surface facing ~~said the~~ active surface of ~~said the~~ first semiconductor die by aligning a peripheral edge of the at least one second semiconductor die with an alignment structure disposed on the active surface of the first semiconductor die, ~~said the~~ corresponding bond pads of ~~said the~~ first and ~~said the~~ at least one second semiconductor dice in alignment with one another;

electrically connecting at least some bond pads of ~~said the~~ corresponding bond pads via laterally discrete, physically unconnected conductive structures;

electrically connecting bond pads of ~~said the~~ first semiconductor die exposed beyond ~~said the~~ outer periphery of ~~said the~~ at least one second semiconductor die to ~~said the~~ corresponding contacts of ~~said the~~ carrier;

providing a carrier with a plurality of contacts; and

orienting ~~said the~~ first semiconductor die over ~~said the~~ carrier with ~~said the~~ active surface facing ~~said the~~ carrier, bond pads of ~~said the~~ first semiconductor die exposed beyond an outer periphery of ~~said the~~ at least one second semiconductor die in alignment with corresponding contacts of ~~said the~~ carrier.

24. (currently amended) The method of claim 23, further comprising electrically connecting ~~said the~~ plurality of bond pads of ~~said the~~ at least one second semiconductor die to ~~said the~~ corresponding plurality of bond pads of ~~said the~~ first semiconductor die.

25. (canceled)

26. (currently amended) The method of claim 23, further comprising disposing a quantity of encapsulant material over at least ~~said~~ the active surface of ~~said~~ the first semiconductor die.

27. (currently amended) The method of claim 26, wherein ~~said~~ disposing ~~said~~ the quantity of encapsulant material comprises disposing underfill material between ~~said~~ the first semiconductor die and ~~said~~ the carrier.

28. (currently amended) The method of claim 26, wherein ~~said~~ disposing ~~said~~ the quantity of encapsulant material comprises substantially covering at least ~~said~~ the first semiconductor die.

29. (currently amended) The method of claim 23, wherein ~~said~~ providing ~~said~~ the carrier comprises providing a carrier substrate with ~~said~~ the plurality of contacts comprising contact pads located on a surface thereof.

30. (currently amended) The method of claim 29, wherein ~~said~~ providing ~~said~~ the carrier substrate comprises providing a carrier substrate with at least one recess formed in ~~said~~ the surface.

31. (currently amended) The method of claim 30, wherein ~~said~~ orienting ~~said~~ the first semiconductor die comprises at least partially disposing ~~said~~ the at least one second semiconductor die within ~~said~~ the at least one recess.

32. (currently amended) The method of claim 23, wherein ~~said~~ providing ~~said~~ the carrier comprises providing a plurality of leads, each of ~~said~~ the plurality of leads corresponding to ~~said~~ the bond pads of ~~said~~ the first semiconductor die exposed beyond ~~said~~ the outer periphery of ~~said~~ the at least one second semiconductor die.

33. (currently amended) The method of claim 29, wherein:  
~~said~~ the providing ~~said~~ the first semiconductor die comprises providing ~~said~~ the first semiconductor die with a first member of a conductive element secured to each bond pad thereof that is located beyond ~~said~~ the outer periphery of ~~said~~ the at least one second semiconductor die; and  
~~said~~ the providing ~~said~~ the carrier substrate comprises providing ~~said~~ the carrier substrate with a second member of ~~said~~ the conductive element secured to each corresponding contact pad thereof.

34. (currently amended) The method of claim 33, further comprising aligning at least ~~said~~ the first and second members of ~~said~~ the conductive element.

35. (currently amended) The method of claim 34, further comprising securing at least ~~said~~ the first and second members of ~~said~~ the conductive element directly to each other.

36. (currently amended) The method of claim 33, further comprising providing a conductive mating structure bearing a third member of ~~said~~ the conductive element between ~~said~~ the first semiconductor die and ~~said~~ the carrier substrate.

37. (currently amended) The method of claim 36, further comprising aligning ~~said~~ the first, second, and third members of ~~said~~ the conductive element.

38. (currently amended) The method of claim 37, further comprising securing ~~said~~ the first, second, and third members of ~~said~~ the conductive element to one another.

39. (currently amended) A method for packaging a semiconductor device assembly, comprising:

providing at least a first multi-chip module including:

a first semiconductor die with a plurality of bond pads arranged in an array over an active surface thereof; and

at least one second semiconductor die including a plurality of bond pads arranged on an active surface thereof, at least one peripheral edge of the at least one second semiconductor die aligned with an alignment structure disposed on the active surface of the first semiconductor die, each of ~~said the~~ plurality of bond pads of ~~said the~~ at least one second semiconductor die in alignment with corresponding bond pads of ~~said the~~ first semiconductor die, other bond pads of ~~said the~~ first semiconductor die being exposed beyond an outer periphery of ~~said the~~ at least one second semiconductor die, ~~said the~~ active surfaces of ~~said the~~ first semiconductor die and ~~said the~~ at least one second semiconductor die facing one another, and ~~said the~~ bond pads of ~~said the~~ at least one second semiconductor die electrically connected to ~~said the~~ corresponding bond pads of ~~said the~~ first semiconductor die, other bond pads of ~~said the~~ first semiconductor die exposed laterally beyond an outer periphery of ~~said the~~ at least one second semiconductor die, ~~at least some bond pads of at least one of said first semiconductor die and said at least one second semiconductor die being recessed;~~

providing a carrier including contacts; and

orienting ~~said the~~ at least ~~said the~~ first multi-chip module with ~~said the~~ active surface of ~~said the~~ first semiconductor die facing ~~said the~~ carrier and ~~said the~~ other bond pads in alignment with corresponding contacts of ~~said the~~ carrier.

40. (currently amended) The method of claim 39, further comprising:

providing at least a second multi-chip module including:

another first semiconductor die with a plurality of bond pads arranged in an array over an active surface thereof; and

an another at least one second semiconductor die including a plurality of bond pads arranged on an active surface thereof, each of ~~said the~~ plurality of bond pads of

~~said~~ the another at least one second semiconductor die in alignment with corresponding bond pads of ~~said~~ the another first semiconductor die, ~~said~~ the active surfaces of ~~said~~ the another first semiconductor die and ~~said~~ the another at least one second semiconductor die facing one another, and ~~said~~ the bond pads of ~~said~~ the another at least one second semiconductor die electrically connected to ~~said~~ the corresponding bond pads of ~~said~~ the another first semiconductor die, other bond pads of ~~said~~ the another first semiconductor die exposed laterally beyond an outer periphery of ~~said~~ the another at least one second semiconductor die; and

orienting ~~said~~ the another at least ~~said~~ the second multi-chip module over ~~said~~ the carrier with ~~said~~ the active surface of ~~said~~ the another first semiconductor die facing ~~said~~ the carrier and ~~said~~ the other bond pads in alignment with corresponding contacts of ~~said~~ the carrier.

41. (currently amended) The method of claim 12, further comprising:  
positioning a cover over ~~said~~ the first semiconductor device and ~~said~~ the at least one second semiconductor device.

42. (currently amended) The method of claim 1, wherein at least one of ~~said~~ providing ~~said~~ the first semiconductor die and ~~said~~ providing ~~said~~ the at least one second semiconductor die comprises providing at least one semiconductor die with at least some of ~~said~~ the bond pads thereof being exposed through alignment recesses in an active surface thereof.

43. (currently amended) The method of claim 39, wherein:  
~~said~~ providing ~~said~~ the carrier comprises providing a carrier including a recess with a ledge therein and contacts exposed at ~~said~~ the ledge; and  
~~said~~ orienting comprises orienting ~~said~~ the at least ~~said~~ the first multi-chip module within ~~said~~ the recess with ~~said~~ the active surface of ~~said~~ the first semiconductor die facing ~~said~~ the carrier and ~~said~~ the ledge.

44. (currently amended) The method of claim 43, further comprising:  
positioning a cover over ~~said~~ the recess and ~~said~~ the first and at least one second semiconductor dice therein.